Review for Single Electron Transistor

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Abstract Single electron transistor (SET) is a novel idea and has been intensively studied. This review gives a general picture of SET, such as its mechanism, fabrication, application and problems faced.
Key words SET quantum dot tunneling Chemical self-assembly

During 1980s, the main discoveries in mesoscopic physics are the tunneling of single electron and Coulomb blockade phenomena[1,2,13], which make many scientists predict that if the size of the quantum dots is reduced to several nanometers, it is highly possible to produce applicable single electron transistor (SET) which works above liquid nitrogen temperature, and this will bring a revolution to electronic science. Since then SET has been a hot research area. The breakthrough of nanotech as well as its successful combination with semiconductor technologies gives hope to SET, and some think that it will be a mature technique in the coming decade.

1 Mechanism of SET

Usually electrons move continuously in the common transistors, but as the size of the system goes down to nanoscale (for example, the size of metal atoms can be several nm, and the size of semi-conductive particles can be several tens nm), the energy of the system is quantumized, that is, the process of charging and discharging is discontinuous. The energy for one electron to move into the system is:

$$Ec = e^2 / 2C$$

where C is the capacitance of this system. This Ec is called Coulomb blockade energy, which is the repelling energy of the previous electron to the next electron. For a tiny system, the capacitance C is very small, thus Ec can be very high, and the electrons cannot move simultaneously, but must pass through one by one. This phenomenon is called "Coulomb blockade", and has been observed in 1980s.

If two quantum dots(QD) are joined at a point and form a channel, it is possible for an electron to pass from one dot over the energy barrier and move to the other dot, this is called "tunneling phenomenon". In order to overcome the barrier (Ec), the applied voltage on the quantum dots (V/2) should be

$$V > e/C$$

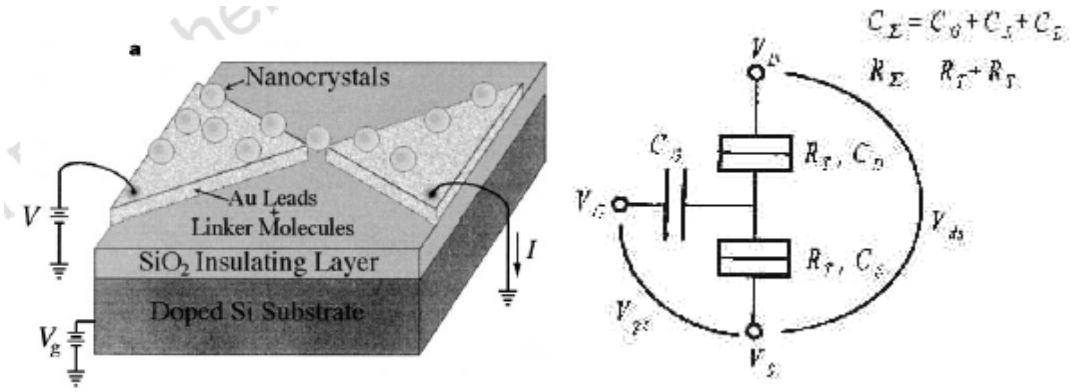
In order to observe Coulomb blockade and tunneling, the energy an electron assumes must be higher than the thermal scattering energy, that is

$$e^2 / 2C > k_B T$$

where k_B is the Boltzman constant.
As this equation predicts, if the capacitance is low enough, that is, if the size of the QDs can be reduced to several nm, Coulomb blockade and tunneling can be observed at high (room) temperature.
If the two QDs are joined respectively with other conductive materials such as metal wires or conductive polymer leads, a SET is formed. A model of SET is shown in Fig.1, (b) is the simplified model. The two areas filled with patched pattern are tunneling

junctions; there are some discrete Coulomb islands between them. R1, C1 and R2, C2 are the resistance and capacitance of the junctions. The junctions form the source and drain of the transistor, $\pm V/2$ voltages are applied to them through conductive wires, the tunneling current pass through the islands is I. A layer of insulating media separates the islands from the gate; the capacitance between them is Cg. A voltage of Vg is applied on the gate and controls the open or close of the SET.

Because of its unique structure, SET has many prospective characteristics such as low power consumption, high sensitivity, high switching speed, high packet density, etc. So much attention has been attracted on their fabrication and industrial realization.



(a) (b)

Fig. 1 a) schematic diagram of SET b) a schematic circuit of SET[9]

2 Fabrication of SET

But the fabrication of SET promotes many difficulties. For SET to be used in a large scale industrially, these factors must be considered:

- It's vitally important to develop technologies for forming nanoscale QDs and quantum wires, which are coupled together through tunneling barrier, and which must be precisely controlled in their size and position.
- Process induced damage and contamination must be avoided in the fabrication of large scale SET circuits.
- The technique must have high reproducibility and controllability.

Basically the fabrication methods can be divided as physical or chemical techniques according to the main procedures.

The physical methods often utilize the combination of thin film and lithographic technologies. Devices with carefully tailored geometries and electron density are got. For example, quantum dots or quasi-zero-dimensional puddles of electrons with weak coupling to simultaneously patterned electrical leads are fabricated to form a SET. However, lithographic and materials limitations restrict the minimum size and composition of such dots (100nm), and studies are typically limited to sub-Kelvin temperatures.

Another approach is to grow nanostructures chemically. [1,2]This approach is prosperous for its low cost and good controllability of the size of Coulomb islands, and it is possible to be a prospective technique. Though this technique is not mature industrially, the SETs fabricated in laboratories show fascinating results. Generally there are three most

important steps: first, the fabrication of Coulomb islands as well as the control of their size and dispersity; second, the formation of tunneling junctions at the joint of electrodes and Coulomb island; third, the formation of gate between substrate and Coulomb islands. The picture below is an example. First, an insulating layer (SiO2) 100nm thick is formed on the Si substrate (or TiO2 on $\alpha - Al_2O_3$), then Au leads are arranged on the substrate by optical lithography coupled with shadow evaporation. Nanocrystals are then attached to the Au leads via a bifunctional linker molecule, forming the Coulomb islands. The nanocrystals used by Klein etc. are Au and CdSe of 5.8nm in diameter. Figure 2 shows the curve they got for measured current I and source-drain bias Vsd at 77K. A coulomb staircase is observed, due to the incremental charging of the dot by single electrons with increasing Vsd, which is characteristic for SET.

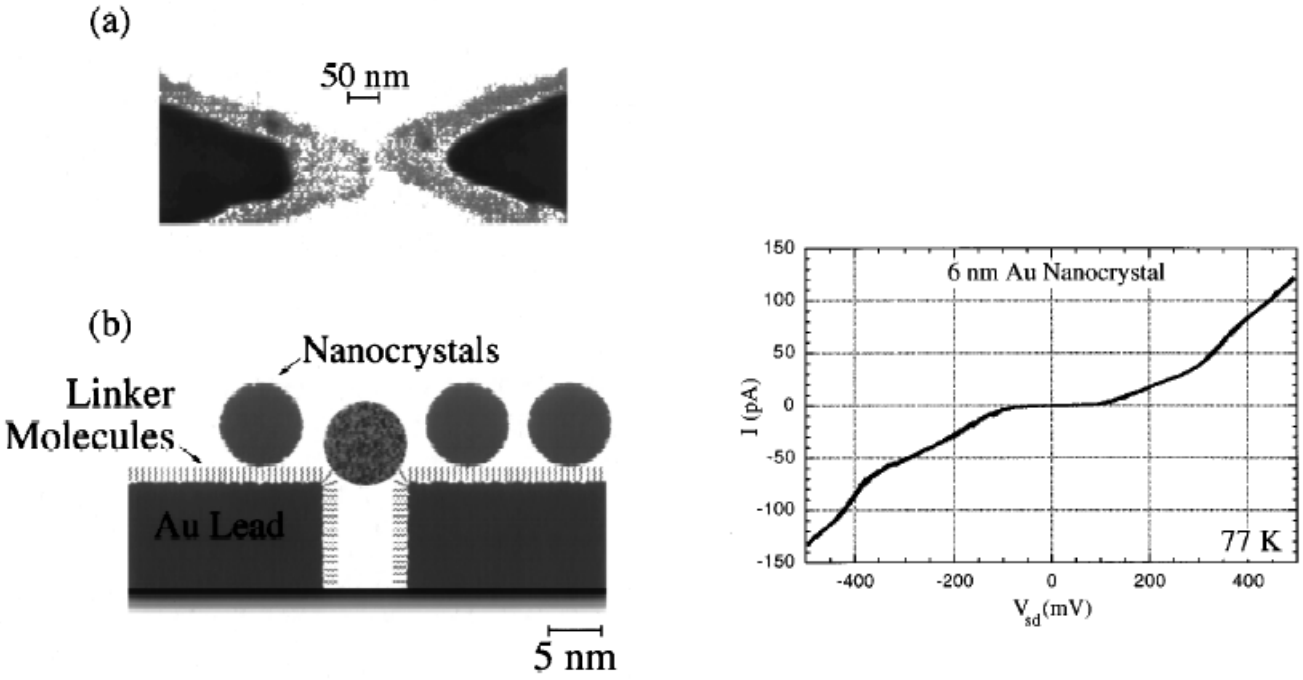


Fig. 2 a) Field emission scanning electron micrograph of a lead structure before nanocrystals are introduced. The light gray region (10nm) is formed by the angle evaporation, the darker region (70nm) is from a normal angle evaporation. b) Schematic cross section of nanocrystals bound via a bifunctional linker molecule to the leads.
d) I-Vsd characteristic of a 5.8nm diam Au nanocrystal measured at 77K.

Atomic force microscopy (AFM) nano-oxidation process [3]

Yoshitaka etc. developed a method to use AFM to fabricate SET. $\alpha - Al_2O_3$ is used as the substrate, a layer of Ti is deposit on the substrate. As a pulse bias is applied between the SFM top and the surface of Ti metal film, the moisture in the ambient air is decomposed and a TiOx line of 15~25nm is formed by chemical reaction. These lines work as the tunnel junctions. The fabricated SET consists of one island sandwiched

between two tunnel junctions. The island width is about 8nm. Typical Coulomb oscillation is observed in this SET, with the period about 2V.
The advantage of AFM is the controllability of size and position in the viewpoint of nanofabrication. But the shortage of this method is it is not so suitable for fabricating large quantities.

In order to optimize the device properties, the reproducible structure of Si-based SETs are substantially studied. Its advantage is that the size of Si islands can be geometrically well controlled because of the advance of modern semiconducting technologies. A side-wall patterning method is proposed. This is based on a silicon-on-insulator (SOI) quantum wire and an electrostatically defined island beyond the limit of lithography resolution. This method takes the advantage of the good selectivity in reactive-ion plasma between Si and SiO2, and finally a 30nm-wide quantum wire is formed, and then poly-Si sidewall depletion gate is formed between these wires, this depletion areas work as Coulom islands. The characteristic I-V curve is observed for this system. This method is very prospective for the possibility of large scale of fabricating SETs.[15]

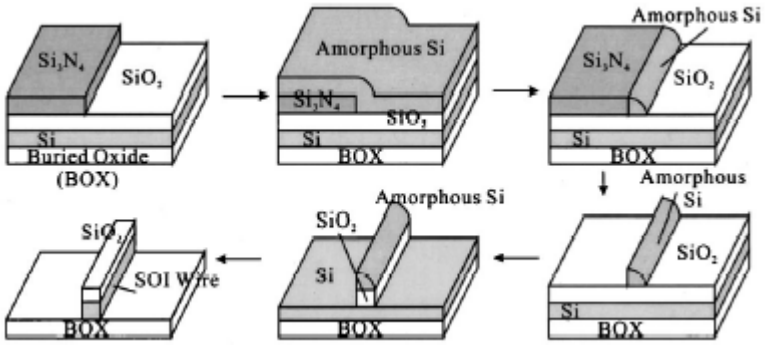


Fig. 3[4] Schematics of the process sequence of side-wall patterning method

3 Applications
Because of its small size, low energy consumption and high sensitivity, SET has found many applications in many areas. What's most exciting is the potential to fabricate them in large scale and use them as common units in modern computer and electronic industry.

Single electron memory[11]
Scientists have long been endeavored to enhance the capacity of memory devices. If single electron memory can be realized, the memory capacity is possible to reach its utmost limit. SET can be used as memory cell since the state of Coulomb island can be changed by the existence of one electron. Chou and Chan [5] first pointed out the possibility of using SET as memories in which information is stored as the presence or absence of a single electron on the cluster. They fabricated a SET by embedding one or several nano Si powder in a thin insulating layer of SiO2, then arranging the source and drain as well as gate around this Coulomb island. The read/write time of Chan's structure is about 20ns, lifetime is more than 10^9 cycles, and retention time (during which the electron trapped in the island will not leak out) can be several days to several weeks. These parameters would satisfy the standards of computer industry, so SET can be

developed to be a candidate of basic computer units. If a SET stands for one bit, then an array of 4~7 SETs will be substantial to memorize different states. The properties of the memory unit composed of SETs are far more advantageous than that of CMOS. But the disadvantage is the practical difficulty in fabrication. When the time comes for the large scale integration of SETs to form logic gates, the full advantages of single electron memory will show. This is the threshold of quantum computing.

High sensitivity electrometer

The most advanced practical application currently for SETs is probably the extremely precise solid-state electrometers (a device used to measure charge). The SET electrometer is operated by capacitively coupling the external charge source to be measued to the gate. Changes in the SET source-drain current are then measured. Since the amplification coefficient is very big, this device can be used to measure very small change of current. Experiments showed that if there is a charge change of e/2 on the gate, the current through the Coulomb island is about 10^9 e/sec. This sensitivity is many orders of magnitude better than common electrometers made by MOSFIT. SETs have already been used in metrological applications as well as a tool for imaging localized individual changes in semiconductors. Recent demonstration of single photon detection [6] and rf operation [7] of SETs make them exciting for new applications ranging from astronomy to quantum computer read-out circuitry.

The SET electrometer is in principle not limited to the detection of charge sites on a surface, but can also be applicable to a wide range of sensitive chemical signal transduction events as well. For example, the gate can be made coupling with some molecules, thus can measure other chemical properties during the process.

However, as Lewis K M etc. pointed out [8], SETs electrometer must be designed with care. If the device under test has a large capacitance, it is not advantageous to use SETs as an electrometer. Since for a typical SET, $C_{SET} < 1\mu F$, the suppression factor becomes unacceptable when the macroscopic device has a capacitance in the pF or nF range. Therefore, SET amplifiers are not currently used for measuring real macroscopic devices. Other low-capacitance electrometers such as a recently proposed quantum point contact electrometer also suffer from a similar capacitance mismatch problem. But it is believed that if the capacitance mismatch can be solved efficiently, SETs may find many new ultra low-noise analog applications.

Microwave detection

If a SET is attacked black body radiation, the photon-aided tunneling will affect the charge transfer of the system. Experiments show that the electric character of the system will be changed even by a tiny amount of radiation. The sensitivity of this equipment is about 100 times higher than the current best thermal radiation detector.

4 Main problems facing the application of SET

a Integration of SETs in a large scale

As has been mention above, to use SETs at room temperature, large quantities of monodispersed nanoparticles less than 10nm in diameter must be synthesized. it is very

hard to fabricate large quantities of SETs by traditional optical lithography and semiconducting process. Chemical self-assembly has the potential to solve this problem. This method adopts the metal-organic precursors and deposits nano clusters on the substrate. But the position cannot be decisively control and it's not a mature technology. The large quantity integration of SETs depends greatly on the development of semiconducting industry of nanotech.

b Linking SETs with the outside environment

Methods must be developed for connecting the individual structures into patterns which function as logic circuits, and these circuits must be arranged into larger 2D patterns. There are two ideas. One is by doping, that is, integrating SET as well as related equipments with the existed MOSFIT, this is attractive because it can increase the integrating density. The other is to give up linking by wire, instead utilizing the static electronic force between the basic clusters to form a circuit linked by clusters, which is called quantum cellular automata (QCA). Many have tried to use carbon nanotube[12] as leads between a serial of insulating nanoclausters. The state of "0" and "1" can be given by polarization direction affected by applied voltage. Complex analog circuits can be made by QCA. The advantage of QCA is its fast information transfer velocity between cells (almost near optic velocity) via electrostatic interactions only, no wire is needed between arrays and the size of each cell can be as small as 2.5nm, this made them very suitable for high density memory and the next generation quantum computer.

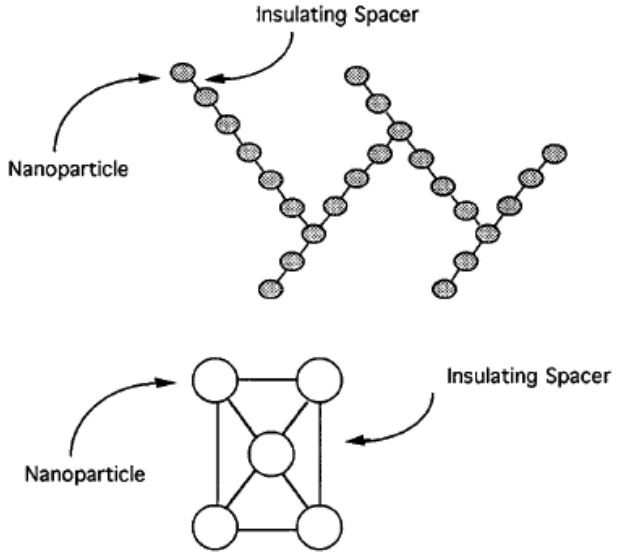


Fig. 4 Nanoparticle–insulator structures proposed in the wireless computing schemes of Korotkov (top) and Lent (bottom). The circles represent quantum dots, the lines are insulating spacers.[5]

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